

WHAT IS CLAIMED IS:

- 1           1. An integrated circuit comprising a first impedance termination circuit,  
2 the first impedance termination circuit comprising:
  - 3           a first termination resistor coupled to a first input/output pin on the integrated  
4 circuit;
  - 5           a common mode driver; and
  - 6           a first transistor coupled between the first termination resistor and the common  
7 mode driver, the first transistor blocking current flow through the first termination resistor  
8 when the first transistor is OFF,  
9           wherein a body of the first transistor is coupled to a first supply voltage.
- 1           2. The integrated circuit according to claim 1 further comprising:  
2           a second transistor coupled in parallel with the first transistor that blocks  
3 current flow through the first termination resistor when the first and the second transistors are  
4 OFF,  
5           wherein a body of the second transistor is coupled to a second supply voltage.
- 1           3. The integrated circuit according to claim 1 wherein the first impedance  
2 termination circuit further comprises:  
3           a first pass gate coupled in parallel with the first termination resistor.
- 1           4. The integrated circuit according to claim 3 wherein the first  
2 termination impedance circuit further comprises:  
3           a second pass gate coupled in parallel with the first termination resistor and  
4 the first pass gate.
- 1           5. The integrated circuit according to claim 3 wherein a second  
2 termination resistor is coupled in series with the first termination resistor and the first pass  
3 gate.
- 1           6. The integrated circuit according to claim 1 further comprising a second  
2 impedance termination circuit, the second impedance termination circuit comprising:  
3           a second termination resistor coupled to a second input/output pin on the  
4 integrated circuit; and

5                   second and third transistors coupled in parallel between the second termination  
6 resistor and the common mode driver, the second and the third transistors blocking current  
7 flow through the second termination resistor when the second and the third transistors are  
8 OFF,

9                   wherein a body of the second transistor is coupled to the first supply voltage,  
10 and a body of the third transistor is coupled to a second supply voltage.

1                   7.       The integrated circuit according to claim 6 wherein the second  
2 impedance termination circuit further comprises:

3                   first and second pass gates coupled in parallel with the second termination  
4 resistor; and

5                   a third termination resistor coupled in series between the second termination  
6 resistor and the second pin.

1                   8.       The integrated circuit according to claim 6 further comprising a third  
2 impedance termination circuit, the third impedance termination circuit comprising:

3                   a third termination resistor coupled to the first input/output pin; and

4                   fourth and fifth transistors coupled in parallel between the third termination  
5 resistor and the common mode driver, the fourth and the fifth transistors blocking current  
6 flow through the third termination resistor when the fourth and the fifth transistors are OFF,

7                   wherein a body of the fourth transistor is coupled to the first supply voltage,  
8 and a body of the fifth transistor is coupled to the second supply voltage.

1                   9.       The integrated circuit according to claim 8 further comprising a fourth  
2 impedance termination circuit, the fourth impedance termination circuit comprising:

3                   a fourth termination resistor coupled to the second input/output pin; and

4                   sixth and seventh transistors coupled in parallel between the fourth termination  
5 resistor and the common mode driver, the sixth and the seventh transistors blocking current  
6 flow through the fourth termination resistor when the sixth and the seventh transistors are  
7 OFF,

8                   wherein a body of the sixth transistor is coupled to the first supply voltage,  
9 and a body of the seventh transistor is coupled to the second supply voltage.

1                   10.      The integrated circuit according to claim 1 wherein the integrated  
2 circuit is a field programmable gate array.

1                   11.    A method for providing termination impedance to a first pin using a  
2 first termination resistor on an integrated circuit, the method comprising:

3                   turning OFF a first pass gate to block current through the first termination  
4 resistor on the integrated circuit, wherein the first pass gate includes first and second  
5 transistors;

6                   driving a voltage on the first pin to high and low supply voltages while the  
7 first pass gate is OFF; and

8                   preventing leakage current from flowing through drain/source-to-body diodes  
9 of the first and the second transistors while the first pass gate is OFF.

1                   12.    The method as defined in claim 11 wherein preventing the leakage  
2 current from flowing further comprises:

3                   coupling a body region of the first transistor to the high supply voltage and a  
4 body region of the second transistor to the low supply voltage.

1                   13.    The method as defined in claim 11 further comprising:

2                   turning ON the first pass gate to provide a current path through the termination  
3 resistors; and

4                   turning ON a second pass gate coupled in parallel with the first termination  
5 resistor.

1                   14.    The method as defined in claim 13 further comprising:

2                   turning ON a third pass gate coupled in parallel with the first termination  
3 resistor, wherein a second termination resistor is coupled between the first pin and the first  
4 termination resistor.

1                   15.    The method as defined in claim 11 further comprising:

2                   turning OFF a second pass gate to block current through a second termination  
3 resistor on the integrated circuit, wherein the second termination resistor provides termination  
4 impedance to a second pin, and the first pass gate includes third and fourth transistors;

5                   driving a voltage on the second pin to the high and the low supply voltages  
6 while the second pass gate is OFF; and

7                   preventing leakage current from flowing through drain/source-to-body diodes  
8 of the third and the fourth transistors while the second pass gate is OFF.

1                   16.     The method as defined in claim 15 wherein the first and the second  
2     pass gates are coupled to a common mode driver.

1                   17.     The method as defined in claim 15 wherein preventing the leakage  
2     current from flowing through the third and the fourth transistors further comprises:  
3                   coupling a body region of the third transistor to the high supply voltage and a  
4     body region of the fourth transistor to the low supply voltage.

1                   18.     A method for providing termination impedance on an integrated  
2     circuit, the method comprising:

3                   providing a current path through a first on-chip resistor to a pin of the  
4     integrated circuit;  
5                   blocking current flow through the first on-chip resistor by turning OFF a first  
6     transistor; and  
7                   preventing source/drain-to-body diodes of the first transistor from becoming  
8     forward biased in response to voltage changes on the pin.

1                   19.     The method of claim 18 wherein preventing the source/drain-to-body  
2     diodes of the first transistor from becoming forward biased further comprises:  
3                   coupling a body region of the first transistor to a first supply voltage.

1                   20.     The method of claim 19 wherein blocking the current flow through the  
2     first on-chip resistor further comprises:  
3                   turning OFF a second transistor coupled in parallel with the first transistor;  
4     and  
5                   preventing the source/drain-to-body diodes of the second transistor from  
6     becoming forward biased in response to voltage changes on the pin.

1                   21.     The method of claim 20 wherein preventing the source/drain-to-body  
2     diodes of the second transistor from becoming forward biased further comprises:  
3                   coupling a body region of the second transistor to a second supply voltage.